



SHAPING THE NEXT GENERATION OF ELECTRONICS

JUNE 23-27, 2024

MOSCONE WEST CENTER
SAN FRANCISCO, CA, USA

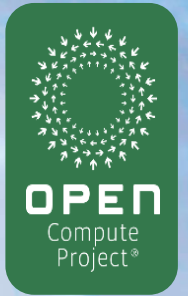




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Open Compute Project

Open Chiplet Economy For AI/HPC

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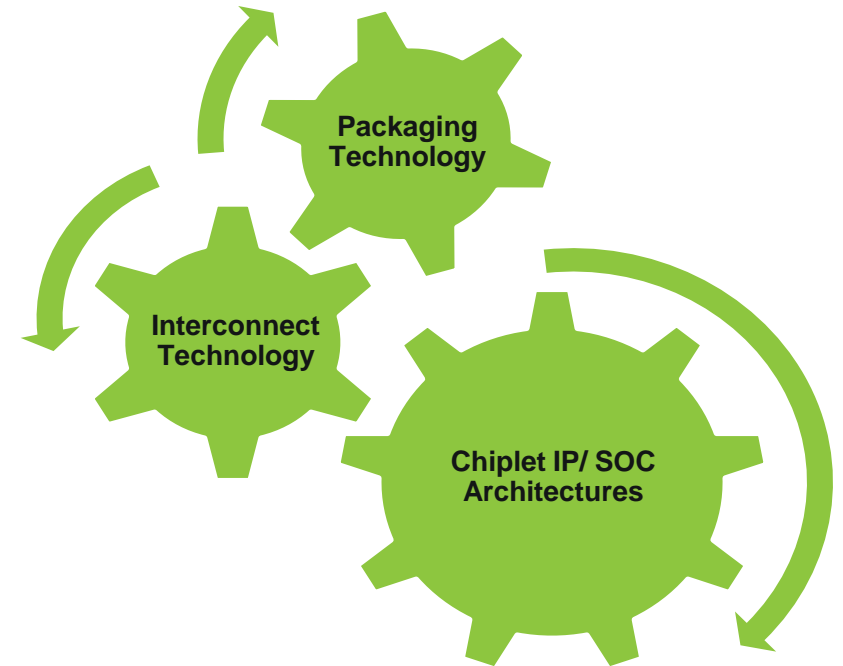


For Open Chiplet Economy...

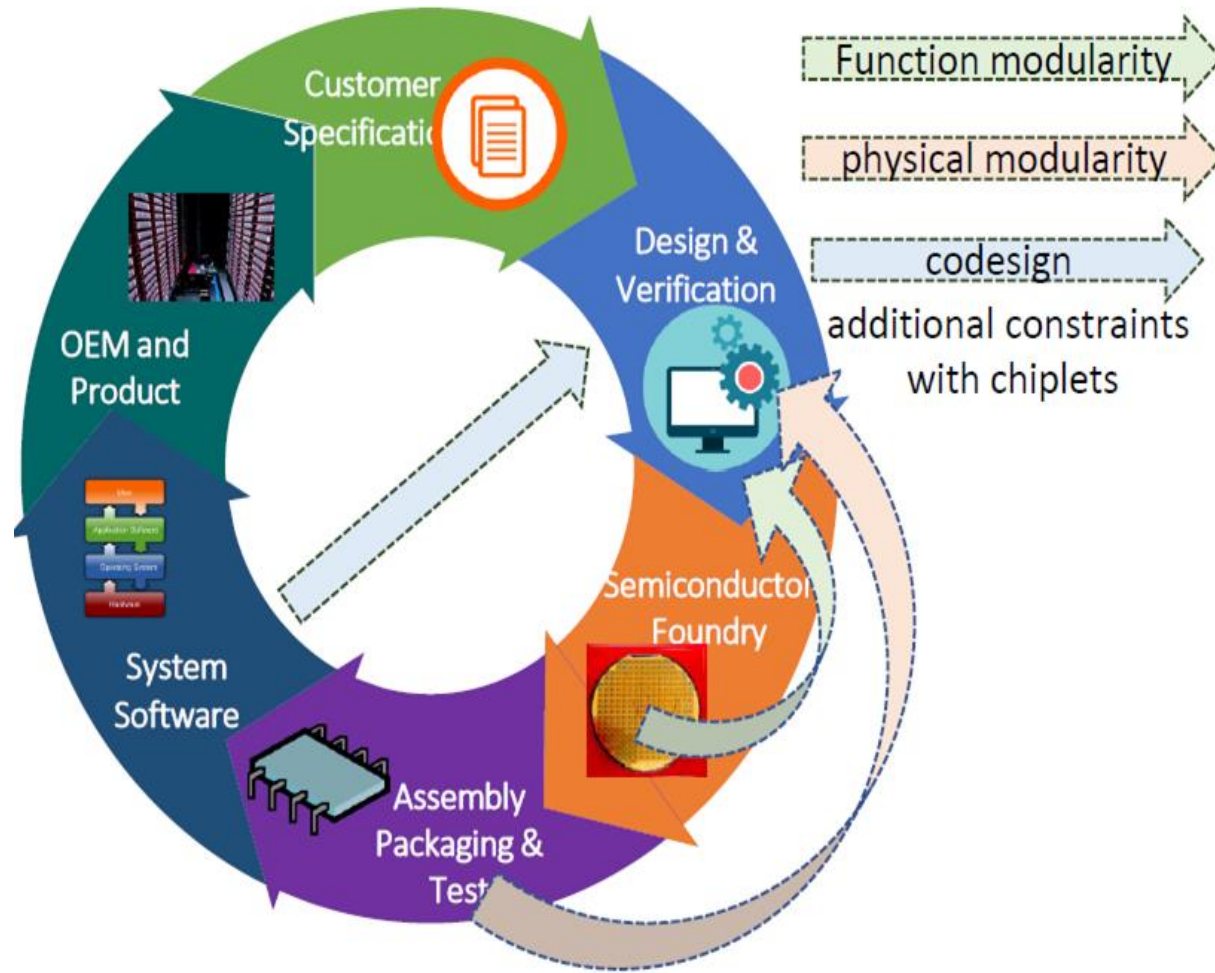
To meet huge diversity in requirements we need

- A core set of application specific standards
- A low barrier to entry for innovation
- Freely customizable for applications

Build and let the market use as it sees fit



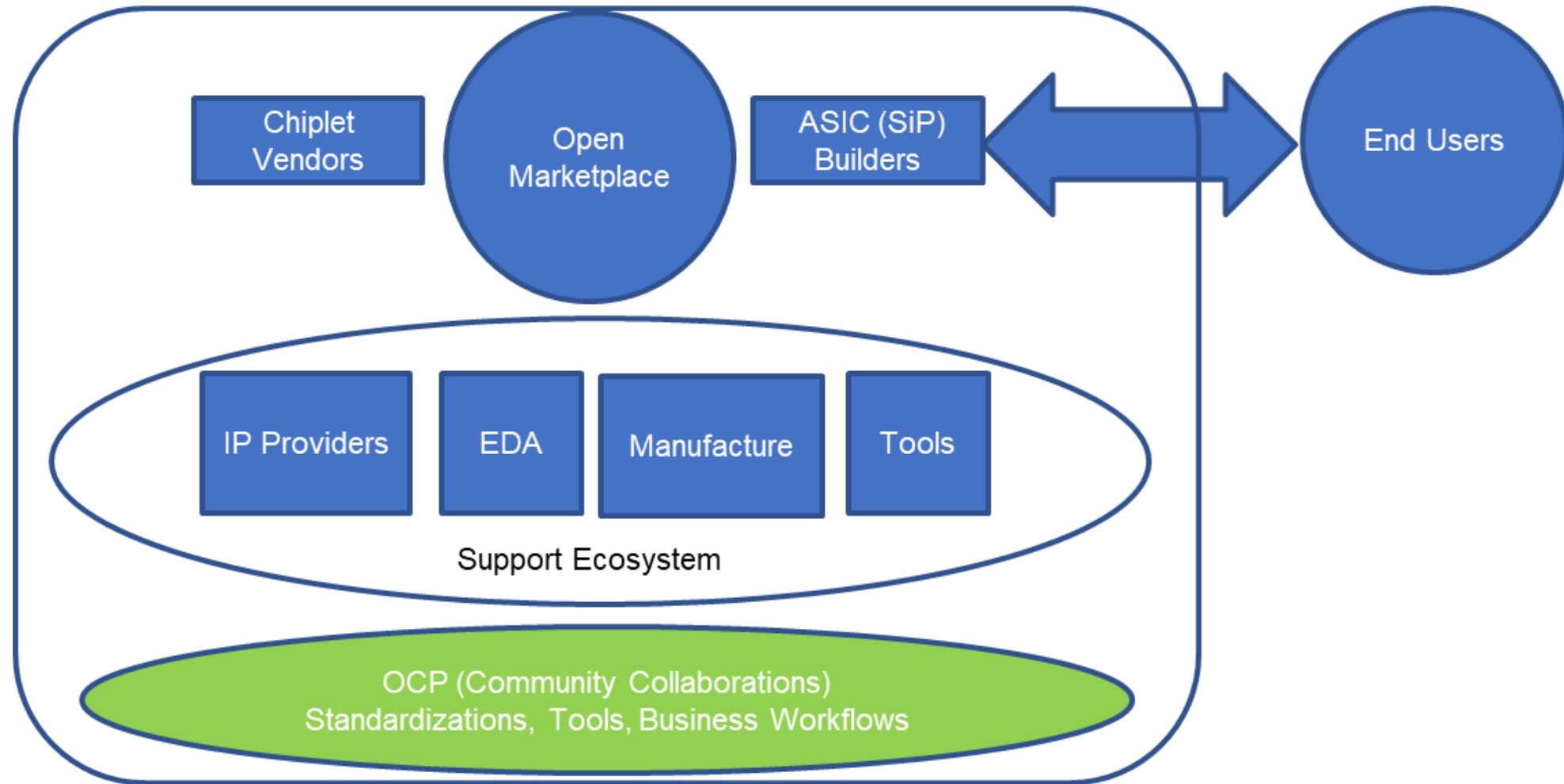
...Need New Integration Across The Value Chain



Factors brought forward or made more complex

- Functional modularity
- Physical modularity
- Interconnect
- Packaging
- Test and operations
- Inventory

Delivered By a New Open Chiplet Economy



Open Chiplet Economy and AI Thrust

Connectivity Chiplets: Co-packaged optics

- Die2Die BoW interconnect standard for Electrical IC
- Co-packaging of optical

Memory Chiplets: HBM

- D2D Memory interconnect
- Co-packaging of memory

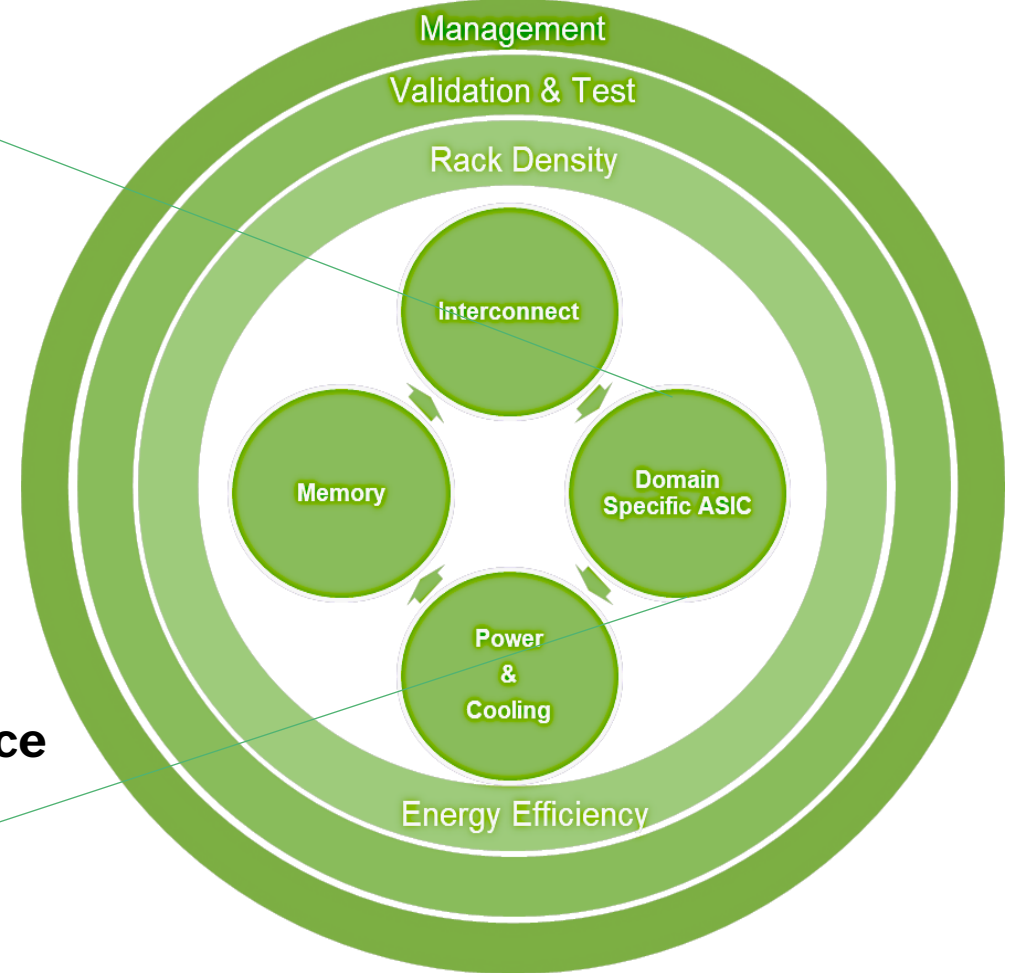
Modular Chiplets: High-performance compute

- Application-driven chiplet modularity standards
- Addressing HPC and AI chiplet needs

Chiplet Modeling: Chiplet design exchange and marketplace

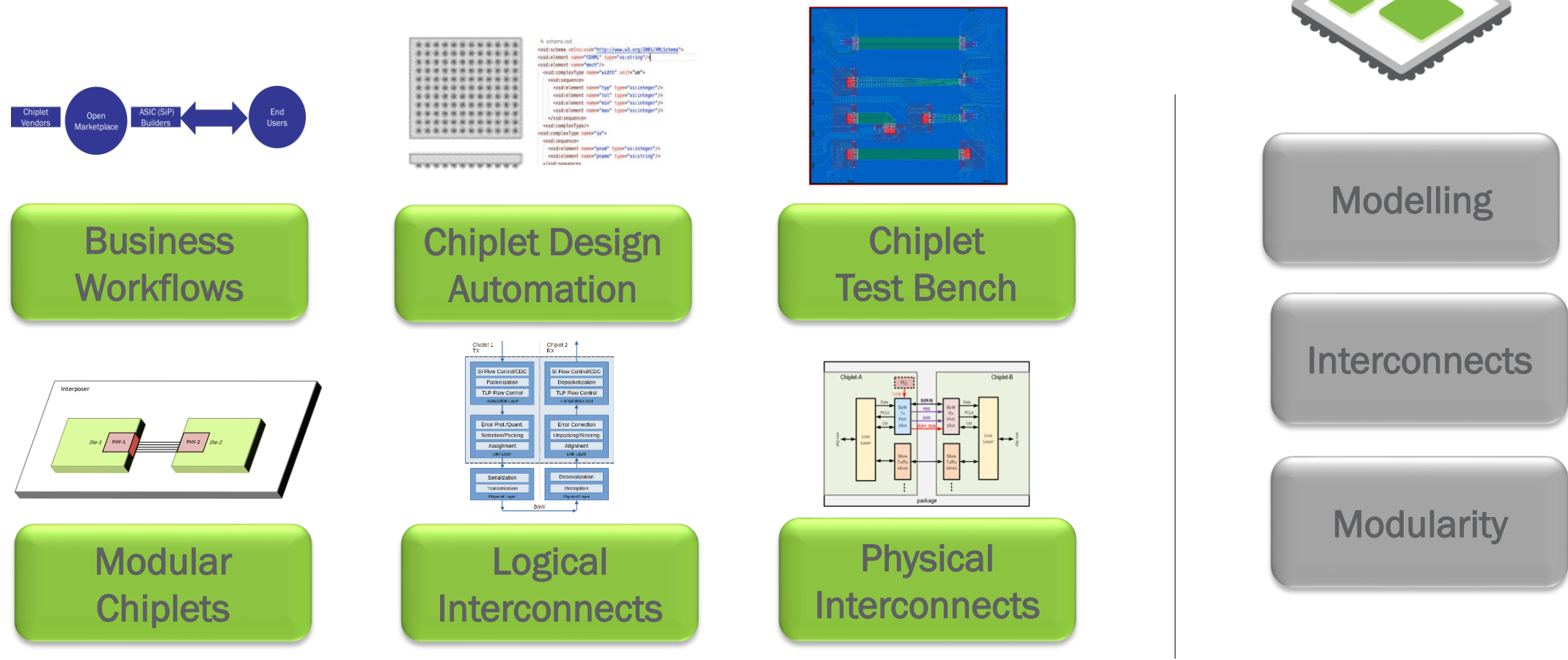
- Seeding the marketplace in collaboration with industry

OCP Open Systems for AI



Open Chiplet Economy Driven By OCP

OCP Open Domain Specific Architecture Project



Get involved!

Join

- Project Mailing Lists
- Project Calls

Drive

- Project Focus
- Thought Leadership

Run

- Project Leaders
- Technical Steering Committee

Contribute

- Specifications
- Products & Facilities

Attend

- OCP Summits
- OCP Panels
- OCP Webinars
- 3rd Party events
- OCP Engineering Workshops
- OCP Events